What is claimed is :

1. A method of driving a liquid crystal display device having a plurality of bus lines for transmitting image data, said method comprising :

branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either said original data rate or a half of said original data rate ;

supplying a source driver circuit with said branched plural-systems image data in synchronizing with at least a clock signal having a clock frequency which is a quarter of said original data rate ; and

allowing said source driver to further branch said branched plural-systems image data into gray scale voltage signals.

2. The method as claimed in claim 1, wherein the number of said systems of said branched plural-systems image data is 2J, where J is a positive integer number.

3. The method as claimed in claim 1, wherein the number of said systems of said branched plural-systems image data is 4J, where J is a positive integer number.

4. The method as claimed in claim 1, wherein said converted data rate is equal to said original data rate.

5. The method as claimed in claim 1, wherein said converted data rate is equal to a half of said original data rate.

6. The method as claimed in claim 1, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and rising edges of said two clock signals serve as triggers to input said image data into said source driver.

7. The method as claimed in claim 1, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and falling edges of said two clock signals serve as triggers to input said image data into said source driver.

8. The method as claimed in claim 1, wherein said at least a clock signal comprises a single clock signal, and both rising edges and falling edges of said single clock signal serve as triggers to input said image data into said source driver.

9. A circuitry for driving a liquid crystal display device, said circuit comprising :

a timing controller for generating image data and at least a clock signal ;

a plurality of data bus lines for transmitting said image data and

at least a clock signal ; and

a plurality of source driver circuits for incorporating said image data in synchronizing with said at least a clock signal and converting said image data into gray scale voltage signals,

wherein said timing controller includes : a branching unit for branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either said original data rate or a half of said original data rate.

10. The circuitry as claimed in claim 9, wherein the number of said systems of said branched plural-systems image data is 2J, where J is a positive integer number.

11. The circuitry as claimed in claim 9, wherein the number of said systems of said branched plural-systems image data is 4J, where J is a positive integer number.

12. The circuitry as claimed in claim 9, wherein said converted data rate is equal to said original data rate.

13. The circuitry as claimed in claim 9, wherein said converted data rate is equal to a half of said original data rate.

14. The circuitry as claimed in claim 9, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and rising edges of said two clock signals serve as triggers to input said image data into said source driver.

15. The circuitry as claimed in claim 9, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and falling edges of said two clock signals serve as triggers to input said image data into said source driver.

16. The circuitry as claimed in claim 9, wherein said at least a clock signal comprises a single clock signal, and both rising edges and falling edges of said single clock signal serve as triggers to input said image data into said source driver.

17. The circuitry as claimed in claim 9, wherein said timing controller further includes :

a data polarity inversion determination unit for verifying whether or not a majority of bits of said branched plural-systems image data is changed in polarity ; and

a data polarity inversion unit for inverting all bits of said branched plural-systems image data in polarity if it is verified that said majority of bits of said branched plural-systems image data is changed in polarity.

18. The circuitry as claimed in claim 17, wherein plural pairs of said data polarity inversion determination unit and said data polarity inversion unit are provided, and the number of said pairs is identical with the number of said systems of said branched plural-systems image data.

19. The circuitry as claimed in claim 17, wherein said data polarity inversion determination circuit further includes :

a polarity change detecting circuit for detecting polarity change in bit unit of said polarity-inverted image data from said branched plural-systems image data ; and

a majority determination circuit for determining whether or not said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data.

20. The circuitry as claimed in claim 9, wherein said timing controller further includes :

a first latch circuit for latching said branched plural-systems image data in synchronizing with said at least a clock signal and outputting said branched plural-systems image data as first output data ;

a first data polarity inversion determination circuit for inverting all bits of said branched plural-systems image data in polarity if a first polarity inversion signal has a predetermined level which indicates polarity inversion, and said first data polarity inversion determination circuit also

outputting polarity-inverted image data ;

a second data polarity inversion determination circuit for comparing said polarity-inverted image data and said branched plural-systems image data to verify whether or not a majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data, and said second data polarity inversion determination circuit also outputting a second polarity inversion signal which has a predetermined level which indicates polarity inversion, if said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data ; and

a second latch circuit for latching said second polarity inversion signal in synchronizing with said at least a clock signal and supplying said first polarity inversion signal to said first data polarity inversion determination circuit.

21. The circuitry as claimed in claim 20, wherein said timing controller further more includes :

a third latch circuit for latching said polarity-inverted image data in synchronizing with said at least a clock signal and supplying said polarity-inverted image data to said source driver ;

a fourth latch circuit for latching said first polarity inversion signal in synchronizing with said at least a clock signal and supplying said first polarity inversion signal to said source driver.

22. The circuitry as claimed in claim 21, wherein plural sets of said first and second data polarity inversion determination circuits and said first to fourth latch circuits are provided, and the number of said pairs is identical with the number of said systems of said branched plural-systems image data.

23. The circuitry as claimed in claim 21, wherein said second data polarity inversion determination circuit further includes :

a polarity change detecting circuit for detecting polarity change in bit unit of said polarity-inverted image data from said branched plural-systems image data ; and

a majority determination circuit for determining whether or not said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data.

24. A timing controller comprising :

a serial-to-parallel converting unit for converting original image data having an original data rate into converted plural-systems image data comprising plural systems having a converted data rate which is equal to either said original data rate or a half of said original data rate ; and

a clock generator for generating at least a clock signal.

25. The timing controller as claimed in claim 24, wherein the number of said systems of said converted plural-systems image data is 2J, where J

is a positive integer number.

26. The timing controller as claimed in claim 24, wherein the number of said systems of said converted plural-systems image data is 4J, where J is a positive integer number.

27. The timing controller as claimed in claim 24, wherein said converted data rate is equal to said original data rate.

28. The timing controller as claimed in claim 24, wherein said converted data rate is equal to a half of said original data rate.

29. The timing controller as claimed in claim 24, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and rising edges of said two clock signals serve as triggers to input said image data into said source driver.

30. The timing controller as claimed in claim 24, wherein said at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and falling edges of said two clock signals serve as triggers to input said image data into said source driver.

31. The timing controller as claimed in claim 24, wherein said at least a clock signal comprises a single clock signal, and both rising edges

and falling edges of said single clock signal serve as triggers to input said image data into said source driver.

32. The timing controller as claimed in claim 24, wherein said serial-to-parallel converting unit further includes :

a data polarity inversion determination unit for verifying whether or not a majority of bits of said converted plural-systems image data is changed in polarity ; and

a data polarity inversion unit for inverting all bits of said converted plural-systems image data in polarity if it is verified that said majority of bits of said converted plural-systems image data is changed in polarity.

33. The timing controller as claimed in claim 32, wherein plural pairs of said data polarity inversion determination unit and said data polarity inversion unit are provided, and the number of said pairs is identical with the number of said systems of said converted plural-systems image data.

34. The timing controller as claimed in claim 32, wherein said data polarity inversion determination circuit further includes :

a polarity change detecting circuit for detecting polarity change in bit unit of said polarity-inverted image data from said converted plural-systems image data ; and

a majority determination circuit for determining whether or not

said majority of bits of said polarity-inverted image data is different in polarity from said converted plural-systems image data.

35. The timing controller as claimed in claim 24, wherein said serial-to-parallel converting unit further includes :

a first latch circuit for latching said converted plural-systems image data in synchronizing with said at least a clock signal and outputting said converted plural-systems image data as first output data ;

a first data polarity inversion determination circuit for inverting all bits of said converted plural-systems image data in polarity if a first polarity inversion signal has a predetermined level which indicates polarity inversion, and said first data polarity inversion determination circuit also outputting polarity-inverted image data ;

a second data polarity inversion determination circuit for comparing said polarity-inverted image data and said converted plural-systems image data to verify whether or not a majority of bits of said polarity-inverted image data is different in polarity from said converted plural-systems image data, and said second data polarity inversion determination circuit also outputting a second polarity inversion signal which has a predetermined level which indicates polarity inversion, if said majority of bits of said polarity-inverted image data is different in polarity from said converted plural-systems image data ; and

a second latch circuit for latching said second polarity inversion signal in synchronizing with said at least a clock signal and supplying said

first polarity inversion signal to said first data polarity inversion determination circuit.

36. The timing controller as claimed in claim 35, wherein said serial-to-parallel converting unit further more includes :

a third latch circuit for latching said polarity-inverted image data in synchronizing with said at least a clock signal and supplying said polarity-inverted image data to said source driver ;

a fourth latch circuit for latching said first polarity inversion signal in synchronizing with said at least a clock signal and supplying said first polarity inversion signal to said source driver.

37. The timing controller as claimed in claim 36, wherein plural sets of said first and second data polarity inversion determination circuits and said first to fourth latch circuits are provided, and the number of said pairs is identical with the number of said systems of said converted plural-systems image data.

38. The timing controller as claimed in claim 36, wherein said second data polarity inversion determination circuit further includes :

a polarity change detecting circuit for detecting polarity change in bit unit of said polarity-inverted image data from said converted plural-systems image data ; and

a majority determination circuit for determining whether or not

said majority of bits of said polarity-inverted image data is different in polarity from said converted plural-systems image data.